

ADVANCES IN POLYCRYSTALLINE THIN-FILM PHOTOVOLTAICS FOR SPACE APPLICATIONS¹

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INTRODUCTION

Polycrystalline, thin-film photovoltaics represent one of the few (if not the only) renewable power sources which has the potential to satisfy the demanding technical requirements for future space applications. The demand in space is for deployable, flexible arrays with high power-to-weight ratios and long-term stability (15-20 years). In addition, there is also the demand that these arrays be produced by scalable, low-cost, high yield, processes. An approach to significantly reduce costs and increase reliability is to interconnect individual cells series via monolithic integration.

Both CIS and CdTe semiconductor films are optimum absorber materials for thin-film n-p heterojunction solar cells, having band gaps between 0.9-1.5 eV and demonstrated small area efficiencies, with cadmium sulfide window layers, above 16.5% (Ref. 1,2,3). Both CIS and CdTe polycrystalline thin-film cells have been produced on a laboratory scale by a variety of physical and chemical deposition methods, including evaporation, sputtering, and electrodeposition. Translating laboratory processes which yield these high efficiency, small area cells into the design of a manufacturing process capable of producing 1-ft² modules however, requires a quantitative understanding of each individual step in the process and its (each step) effect on overall module performance. With a proper quantification and understanding of material transport and reactivity for each individual step, a manufacturing process can be designed that is not "reactor-specific" and can be controlled intelligently with the design parameters of the process.

Development of a thin-film, manufacturing process depends not only on the scalability of the process but on the overall fixed and operating costs, the environmental compatibility (i.e., material utilization/waste minimization with minimal health and safety risks), and the reproducibility/stability of the process. For this reason, the selection of deposition processes at MMC was influenced by: 1) cost; 2) environmental compatibility; and 3) reproducibility/stability of the process. In the development of CdTe and CIS devices at MMC therefore, CdTe films are being deposited by electrodeposition and CIS films are being deposited by DC, cylindrical magnetron sputtering. Both of these processes are scalable, low-cost processes with relatively minimal environmental impact and a discussion of the development of these processes is presented in this paper.

The objective of this paper is to present an overview of the current efforts at MMC to develop large-scale manufacturing processes for both CIS and CdTe thin-film polycrystalline modules. CIS cells/modules are fabricated in a "substrate configuration" by physical vapor deposition techniques and CdTe cells/modules are fabricated in a "superstrate configuration" by wet chemical methods. Both laser and mechanical scribing operations are used to monolithically integrate (series interconnect) the individual cells into modules. Results will be presented at the cell and module development levels with a brief description of the test methods used to qualify these devices for space applications. The approach and development efforts are directed towards large-scale manufacturability of established thin-film, polycrystalline processing methods for large area modules with less emphasis on maximizing small area efficiencies.

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CELL DEVELOPMENT

A part of the development of a commercial scale process for thin-film polycrystalline modules is an understanding of each of the individual processing steps and its correlation to device performance and reliability. In this section, a summary is presented of each of the processing steps for both CIS and CdTe devices.

Copper Indium Diselenide

CIS heterojunction cells are deposited onto flexible or rigid glass substrates in the "substrate configuration"; substrate, molybdenum back contact, CIS absorber, CdS window layer, ZnO transparent conductive oxide, with a metallized top grid contact. Conventional CIS devices have been optimized on molybdenum-coated glass substrates and little has been reported on the performance of CIS films on flexible substrates. The issue of flexible substrate requirements is discussed along with the current approaches and results for producing thin-film CIS

Substrate - For the rigid cells, borosilicate glass is an inexpensive substrate which matches well with the thermal characteristics of the semiconducting layers and is therefore the substrate of choice for a rigid module. Molybdenum can be uniformly sputtered onto glass substrates over 1 ft² areas and depending on the characteristics of the sputtering chamber (i.e., planar or cylindrical cathodes, oxygen level, etc.), the molybdenum will have a surface roughness similar to the glass substrate with a well-defined texture. Surface profile and texture have been observed to have an effect on overall device performance and the selection of the substrate can have an effect on the roughness and texture of molybdenum back contact.

Although flexible substrates offer inherent processing advantages in the development of a commercial scale process as well as meeting technical goals for space applications which are not obtainable with rigid substrates, substrate flexibility adds complexity to the fabrication process. Typical requirements for a flexible substrate in a CIS module would include such things as: 1) surface finish/profile; 2) high temperature stability (up to 550° C); 3) thermal compatibility (CTE); 4) insulating (dielectric breakdown voltage); 5) chemical/vacuum stability; 6) cost and availability; and 7) flexibility versus strength. Each class of materials, whether it be metal, ceramic, or plastic, has certain drawbacks as a flexible substrate although the leading candidates for flexible substrates are polyimide-type plastics, "metal organic-based" flexible glasses, coated metallic foils, and mica sheets.

Results from thermal gravimetric analysis have shown that nearly all the 'high-temperature' plastics tested out-gas to some degree above 400°C (this does not include evaporation of water above 100°C). This not only alters the properties of the material but can effect the adherence of the semiconductor films during deposition. CIS devices have been fabricated on polyimide films although efficiencies were not significant to report.

Because of their mechanical toughness, high temperature stability, cost, and availability, coated and uncoated metallic foils have been used in the development of flexible CIS devices. Unlike the smooth glass substrates which have been used to produce the highest efficiency cells reported by others, metallic foil substrates have a rougher surface profile which can effect device performance.

The differences between molybdenum coatings on the flexible foils and glass substrates were subtle. Peak to valley variations in the surface profile of the metallic foil were on the order of 200 nm whereas

the variation across a typical glass substrate is on the order of 10 nm. The molybdenum back contact films on metallic foils were highly textured with predominantly a (110) peak in the glancing incidence diffraction spectra. In comparison to single crystal molybdenum, the (110) peak of the sputtered molybdenum film on metallic foil broadened and shifted to higher d-spacings (i.e., residual tensile stresses after the molybdenum deposition and selenization processes). Molybdenum films on the glass substrate were also highly oriented although the (211) was the strongest peak and there was not any detectable broadening or shifting of the primary peaks.

Surface texture of the substrate is certainly a factor in the deposition, nucleation, and growth behavior of semiconducting films. This as well as other subtle factors, such as the surface emissivity/absorptivity of the substrate during thermal processing, can effect the photoresponse of a polycrystalline CIS device.

Molybdenum Back Contact - Depending on the substrate, a 200-1,000 nm thick coating of molybdenum is sputtered onto the surface. Substrate temperature, sputter rate and pressure are used to control the adhesion and stress state of the film; oxygen partial pressure is also used as a parameter to control the properties of the molybdenum film. To improve adhesion of the CIS absorber layer, a graded molybdenum structure can be deposited with copper to produce a pure molybdenum layer at the substrate/contact interface and a pure copper layer at the CIS/contact interface (as reported in the literature (Ref. 4), copper at the back surface of CIS would produce a "p+" structure in the CIS absorber layer and improve the ohmic contact).

CIS Absorber Layer - Reproducibility and uniformity of the CIS absorber layer is one of the most important factors in the performance and manufacturability of large-area modules. Since copper, indium, and selenium are three elements with considerably different properties (i.e., melting points, vapor pressures, oxygen solubility, conductivity, etc.), the formation of a single copper indium diselenide phase over large areas, both kinetically and thermodynamically, will depend on the processing order or deposition sequence and the uniformity of the film deposit(s) over large areas. Lateral compositional and thermal gradients across a large area can result in the formation and microsegregation of secondary phases and since these gradients/heterogeneities are not significant in the "through-thickness dominated" growth behavior of a small area, the processing steps to produce high efficiency small area devices may therefore be limited over larger areas.

The approach in the development of a large scale process has been to select processing sequences for CIS which minimize the number of reaction pathways and secondary phase formation while at the same time, select deposition processes for each sequence which are reproducible and scalable. Two of these approaches are: 1) Cu/In Bilayer approach where copper and indium are successively deposited on a molybdenum back contact and then reacted with either elemental selenium or hydrogen selenide vapor; and 2) Selenized Bilayer approach where first, indium and selenium are deposited/reacted to form indium selenide, followed by copper and selenium deposition to form copper selenide, and finally, the two selenized bilayers are reacted to completion in a selenium atmosphere. The Cu/In bilayer is a low temperature (~400°C) approach with a small number of easily controllable, processing steps, demonstrated large-area scalability, and excellent substrate adhesion. Since a number of reaction pathways are possible with this type of approach, stable binary phases (as well as other types of microsegregation) can form along with the copper indium diselenide phase and degrade the performance of a large-area module.

The selenized bilayer approach on the other hand, reduces the total number of possible reaction pathways by the formation of essentially two stable intermediate binary phases which, when reacted to com-

pletion, can only form a single CIS phase (refer to a $\text{Cu}_{(2-x)}\text{Se}/\text{In}_2\text{Se}_3$ binary phase diagram). Although this type of approach minimizes formation of impurities by limiting the number of reaction pathways, the number of processing steps and substrate temperature are increased in comparison to the Cu/In bilayer approach. In addition, reported efficiencies for this type of approach have only been demonstrated on a small scale.

To evaluate emerging CIS technology, Martin Marietta (MMC), in cooperation with the National Renewable Energy Laboratory, designed and fabricated a CIS flight experiment with cells based on NREL's selenized bilayer process which has demonstrated 16.4% efficiency in AM1.5 insolation this year. In this case, gallium was added to the CIS to improve the bandgap as well as efficiency. The experimental array fabricated for the SAMMES flight experiment is scheduled for launch later this year. Active area efficiency for these devices calculated at 13.5% in AM0 as measured by a pulsed solar simulator at Spectrolab during final assembly. It is anticipated that there will be at least one year of data in orbit from this experiment.

CdS Window Layer - A thin, 40-60 nm - thick, CdS film is deposited onto the CIS absorber layer by the chemical bath deposition process. Cadmium to sulfur ratios in solution have been varied between 10 and 50 to optimize both film properties (i.e., adherence and uniformity) and yield from this batch process. Actual deposition occurs at 85°C in a buffered solution between 9.0 and 10.0 pH and processing time is less than 4 minutes. Reproducibility and uniformity of the thin CdS layer have been demonstrated over 1 ft² areas.

ZnO Top Contact - Since the approach for the molybdenum back contact and CIS absorber layers has been to utilize the potential scalability of a cylindrical, DC-magnetron sputtering process, a similar development strategy was used in the case of the ZnO top contact (ZnO can also be deposited by RF sputtering although the results presented in this paper are with a DC power source). ZnO films were sputtered from an 8" diameter, hot pressed target containing 98 w/o ZnO and 2 w/o Al_2O_3 and the transmittance response for a 902.5 nm-thick film is presented in Figure 1(a). The transmittance response for an uncoated substrate is included for reference.

With DC magnetron sputtering of ZnO, film properties are strongly dependent upon both the processing parameters and the target/substrate geometry. To determine the effect of substrate location with respect to the target source, glass witness coupons were positioned at increasing distances from the target source (normal to the target) and at positions away from the center of the target (parallel to the target surface). Results from this series of tests is shown in Figure 1(b) in which the film resistivity is plotted as a function of location relative to the target center. Within the region defined by the "racetrack" of the target (i.e., ~10 cm), the ZnO film resistivities are less than 1×10^{-3} ohm-cm for all but the 10 cm, target-to-substrate distance. In the fabrication of 10 cm x 10 cm CIS device therefore, processing parameters can be varied to first deposit a thin, high resistivity ZnO film on top of the CdS, followed by the low resistance film referred to above.

The "roll-off" in film resistivity for this 8" target occurs at around 15 cm relative to target center and there is a distinct increase in resistivity across the racetrack region. Degradation of film properties in the vicinity of the target racetrack is well documented in the literature and poor resistivities are said to result from bombardment by energetic neutral and negatively charged oxygen atoms. Such bombardment is believed to cause lower carrier mobilities and concentrations through a decrease in grain size, a mixed

crystalline orientation, and a higher defect density. An additional cause for the variations in resistivity may be due to the variations in the aluminum doping density. A plot of atomic ratio of Al/Zn as a function of the location relative to the target center is presented in Figure 2. Based on these results, the increase in resistivity across the racetrack zone correlates with the drop in Al/Zn ratio. By incorporating existing techniques to control neutral and negatively charged oxygen atoms and minimize racetrack effects, ZnO will then be uniformly deposited over a 30 cm diameter by DC magnetron sputtering.

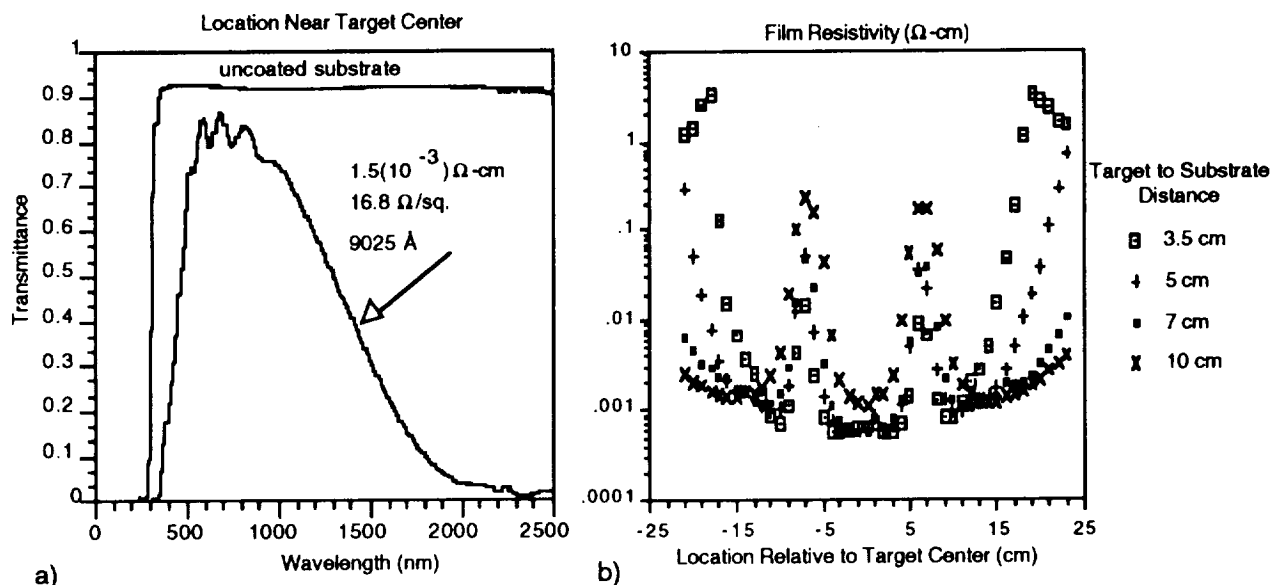


Figure 1 a) Transmittance Spectra for 902.5 nm-Thick ZnO Coating on Glass; b) Film Resistivity as a Function of Distance From the Target Center and Away From the Target

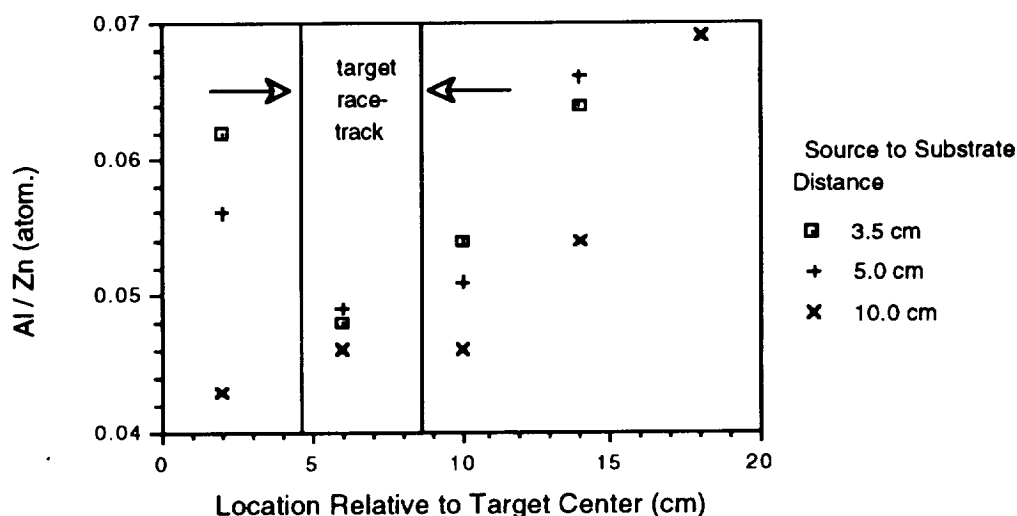


Figure 2 Aluminum/Zinc Ratio (Atomic Percent) as a Function of Distance Away From Target Center (Composition Measured by Wavelength Dispersive X-Ray Spectroscopy (WDS))

Cadmium Telluride

Unlike CIS thin-film devices, CdTe devices are fabricated in the superstrate configuration with entirely wet chemical deposition methods and no vacuum; device structure consists of glass superstrate, transparent conductive oxide, CdS window layer, CdTe absorber, and metal back contact. Using entirely wet chemical processes, thin-film CdTe cells have been fabricated with 6-7% (0.08 cm^2 active area) efficiencies on SnO_2 -coated glass. In this section, a brief overview is presented of the potential scale-up issues related to the CdS solution-growth and CdTe electrodeposition processes.

CdS Window Layer - The CdS deposition process for CdTe thin-film cells is similar to the process for CIS cells in that CdS films are heterogeneously nucleated onto activated surfaces from an aqueous solution containing cadmium salts and thiourea with ammonium as a complexing agent (reaction throttle). For CdTe however, the CdS films are grown on TCO-coated glass substrates with an average thickness between 250 - 320 nm and at a deposition rate of $\sim 180 \text{ nm/hour}$. With a proper selection of the cadmium-to-sulfur ratio and ammonium, which acts as a buffer and a complexing agent for cadmium, film properties can be optimized. CdS quality, in terms of surface adhesion, structure, and yield from a batch process, is directly related to the solubility/precipitation of $\text{Cd}(\text{OH})_2$ and the concentration of unassociated $[\text{Cd}^{2+}]$ cations.

CdS films are reproducibly and uniformly deposited onto 1 ft^2 substrates from a batch, solution-growth process with a $>90\%$ process yield; i.e., minimal waste. For optimum n-type carrier density, proper control of the oxygen/sulfur ratio, and surface activation for the subsequent CdTe electrodeposition step, CdS films are used in the as-deposited condition and are not post heat treated. A typical transmission spectra for CdS on an SnO_2 -coated soda-lime glass is shown in Figure 3. Although there is a shift in the heat treated CdS films to higher wavelengths, the absorption edge for these films is around 520 nm.

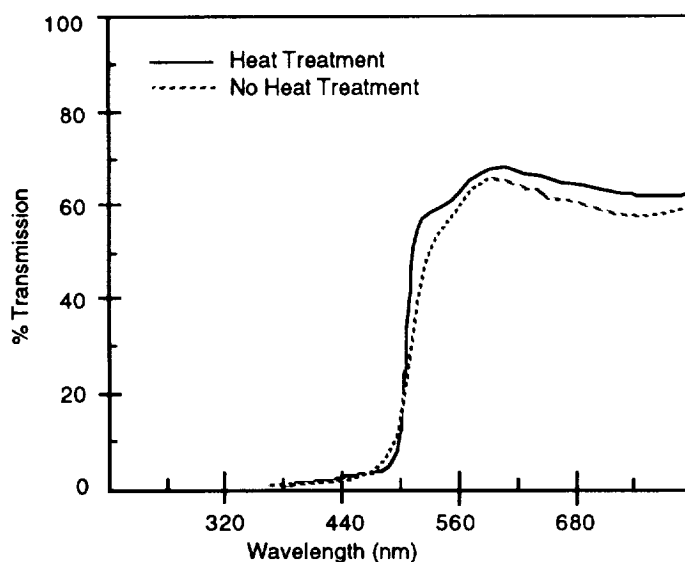


Figure 3 Percent Transmission of Heat Treated and As-Deposited, Solution Grown CdS

CdTe Absorber Layer - Optimally-doped CdTe films are produced by electrodepositing a $1.5 - 2.0 \mu\text{m}$ -thick CdTe layer from an acid bath containing cadmium salts and then heat treating these films at high temperature (400°C) in the presence of CdCl_2 . Although the electrodeposition process was selected

because of its low-cost and potential scalability to larger areas, a number of processing factors, such as cadmium to tellurium ratio in the electrolyte, transport/delivery of cadmium and tellurium to the electrode surface, electrolyte contamination, competing cathodic and anodic reactions, and film resistance of the as-deposited film, can all have a subtle effect on the final electrical quality of the CdTe films (not to mention what effect these factors will have on formation of the n-p junction). In contrast to CdTe films which are deposited by a vacuum, physical vapor deposition process, electrodeposited CdTe films are electrically coupled to the junction partner (i.e., CdS, which is also electrically coupled to a conductive oxide) as electrons are transported through the device during the deposition process. This inherent feature of electrodeposition provides an insitu monitor of CdTe film and device quality and can be used as active feedback control in a commercial scale process.

Through proper control of bath chemistry (pH, cadmium/tellurium ratio, temperature, deposition potential, etc.), CdTe films can be reproducibly deposited over small areas and all of these factors should translate to larger areas, however; as the deposition area increases, film resistivity becomes more critical. Film resistance has a direct effect on the deposition potential which in turn, effects the cadmium to tellurium ratio in the film. With increasing film resistance, the equilibrium potential becomes more noble (positive) and more tellurium is deposited with respect to cadmium. Through-thickness resistivity in the CdS, i.e., from the conductive oxide through the CdS to the CdTe film, is negligible compared to the drop in lateral resistivity which can occur in the TCO over large areas. For example, the voltage drop across a typical 20 ohms/square tin oxide was determined to be ~25 mv/cm. Over a 10 cm area then, the shift in deposition potential would be ~250 mv. A 250 mv shift would correspond to a change in the Cd/Te ratio from 1.0 to a ratio less than 0.8. Without reducing the resistivity of the TCO below 20 ohms/square, uniform films were deposited across 5 cm x 5 cm areas. Although a switch to more conductive TCO films can be made (at the expense of transmittance), lateral film resistivity will still be a significant factor as CdTe devices are fabricated over larger areas.

MODULE DEVELOPMENT

Other than the scaling issues presented above for the cell processing, the remaining issues limiting module and large area array development are the scribing operations which eliminate the hand touch labor of conventional series interconnects and the fabrication of reliable interconnects between modules. Results from the CIS scribing development efforts are presented in this section. A reliable method for bonding interconnects to a molybdenum film has been developed at MMC.

Scribing of the various coating layers of the photovoltaic cells is crucial in the fabrication of monolithically-integrated minimodules. Flow of current occurs from the overlayer transparent conductive oxide (TCO) to the Mo back contact. To enable this current flow in an isolated manner requires the fabrication of scribes in the Mo back contact layer, in the CdS/CIS multilayers to the Mo back contact, and in the ZnO:Al/CdS/CIS multilayers to the Mo back contact. Each of these materials exhibit different thermo-physical properties (absorptance = $f(\text{wavelength } (\lambda))$) and mechanical properties, which affects their removal by scribing processes.

Candidate scribing processes that are being investigated at Martin Marietta include: 1) laser; 2) mechanical; and 3) chemical etching between photolithographically-deposited masks.

For removal of material by laser incidence, critical material properties include absorptance and emittance as a function of wavelength, and melting temperature. For the coatings Mo and CdS/CIS, absorptance generally increases as the incident wavelength is reduced. This suggests the use of lower wavelength lasers, such as a frequency-doubled (or quadrupled) YAG ($\lambda=0.54\text{ }\mu\text{m}$ for frequency-doubled) or excimer lasers will more effectively couple with these coatings, resulting in more efficient coating removal. Care must be exercised, however, not to couple with the underlying substrate material, which may result in substrate damage.

An example of a scribe in a $1\text{ }\mu\text{m}$ Mo coating on glass produced by a Q-switched YAG laser ($\lambda = 1.06\text{ }\mu\text{m}$) is shown in Figure 4(a). In general, the scribe edges appear clean and straight with a small amount of Mo cracking or delamination adjacent to the scribe. Excimer processing also resulted in clean scribe edges, although more cracking and flaking of the Mo was observed. Scribes produced by a pulsed Nd-YAG exhibited some glass substrate cracking and larger berms of material adjacent to the scribe than for the other laser methods.

Laser scribing of the combined CdS/CIS multilayers is more difficult, since the desire is to remove the CdS/CIS layers without damaging the Mo back contact. Of all the laser scribing methods, Excimer laser scribing shows the most promise for selective coating removal. Simple mechanical scribing using a synthetic diamond tool or a stainless steel blade has been found to be more effective for selective removal of CdS/CIS from the Mo back contact. Figure 4b shows an example of a scribe in CdS/CIS which shows removal of the multilayers, without extensive damage to the Mo back contact.

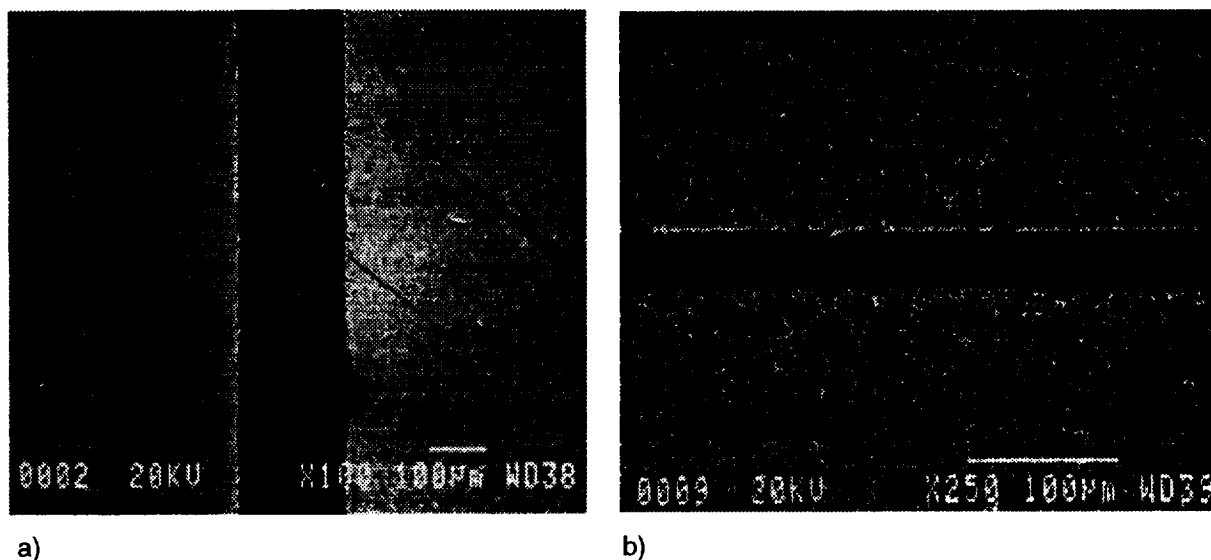


Figure 4 a) SEM Micrograph of Scribe in Mo Coating on Glass Produced by Q-Switched YAG Laser Showing Relatively Clean Scribe Edges and Minor Cracking of Adjacent Mo; b) SEM Micrograph of Scribe in CdS/CIS Coating on Mo-Coated Glass Produced by Mechanical Diamond Scribe Showing Selective Removal of CdS/CIS

QUALIFICATION TESTING

In order to survive the demanding 15-20 year lifetimes in space, thin-film cells and modules need to be first tested in thermal/vacuum and simulated radiation tolerance tests (i.e., solar, electron, proton, etc.). One distinct advantage of CdTe and CIS thin-film polycrystalline devices over silicon and gallium arsenide is the inherent radiation tolerance of the CdTe and CIS semiconducting layers. Long term radiation testing as well as thermal/vacuum cycling of CdTe and CIS cells is in progress.

Just as important as the environmental stability of these devices, however, is the mechanical stability of CdTe and CIS devices and particular, the effect of mechanical forces on the photoresponse of a flexible CIS module. Although preliminary data is available in the literature on the testing of rigid CdTe and CIS thin-film polycrystalline cells in simulated space environments and actual flight experiments, little is known of the effects of mechanical stresses and strains on the electrical behavior of a polycrystalline device. An effort is in progress to test the I-V and spectral response of flexible CIS cells before, during, and after the application of a cyclic bending force.

SUMMARY

An overview of the current efforts at MMC to develop large-scale manufacturing processes for both CIS and CdTe thin-film polycrystalline cells and modules is presented with an emphasis on those issues in each process that are critical to scalability/manufacturability. Except for the CdS window layer, all films in the CIS devices are being deposited by a DC magnetron sputtering system; large-area uniformity was also demonstrated for all the processing steps with the cylindrical magnetron sputtering system. CdTe cells were fabricated entirely by low-cost, wet chemical methods and small area efficiencies on SnO₂-coated soda-lime glass were on the order of 7%. Scalability issues were identified for the CdTe electrodeposition process.

Since a major concern in the fabrication of monolithically integrated modules is the scribing operation, results from laser scribing the CIS back contact and mechanically scribing the CIS/CdS layers are presented. To evaluate emerging CIS technology, Martin Marietta, in cooperation with the National Renewable Energy Laboratory, designed and fabricated a CIS flight experiment with cells based on NREL's selenized bilayer process which has demonstrated 16.4% efficiency in AM1.5 insolation this year.

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